

Description

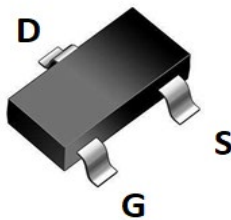
JMT P-channel Enhancement Mode Power MosFET

Features

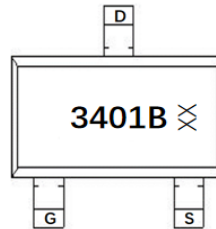
- -30V, -4A
 $R_{DS(ON)} < 64m\Omega @ V_{GS} = -10V$
 $R_{DS(ON)} < 74m\Omega @ V_{GS} = -4.5V$
 $R_{DS(ON)} < 96m\Omega @ V_{GS} = -2.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

Applications

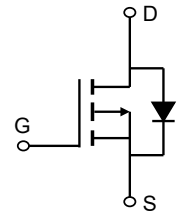
- Load Switch
- PWM Application
- Power Management



SOT-23-3L Top View



Marking and Pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel(pcs)	Per Carton (pcs)
3401B	JMTJ3401B	TAPING	SOT-23-3L	7"	3000	120000

Absolute Maximum Ratings (@ $T_A = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	-30	V
V_{GS}	Gate-to-Source Voltage	± 12	V
I_D	Continuous Drain Current	$T_A = 25^\circ C$	-4
		$T_A = 100^\circ C$	-3
I_{DM}	Pulsed Drain Current ⁽¹⁾	-16	A
P_D	Power Dissipation	$T_A = 25^\circ C$	1.1
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽²⁾	110	$^\circ C/W$
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ C$



Electrical Characteristics (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = -250μA, V _{GS} = 0V	-30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -30V, V _{GS} = 0V	-	-	1.0	μA
I _{GSS}	Gate-Body Leakage Current	V _{DS} = 0V, V _{GS} = ±12V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-0.6	-0.95	-1.3	V
R _{DS(ON)}	Static Drain-Source ON-Resistance ⁽³⁾	V _{GS} = -10V, I _D = -4A	-	49	64	mΩ
		V _{GS} = -4.5V, I _D = -3A	-	57	74	mΩ
		V _{GS} = -2.5V, I _D = -3A	-	74	96	mΩ
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz	-	553	-	pF
C _{oss}	Output Capacitance		-	57	-	pF
C _{rss}	Reverse Transfer Capacitance		-	35	-	pF
Q _g	Total Gate Charge	V _{GS} = 0 to -4.5V V _{DS} = -15V, I _D = -3A	-	6.5	-	nC
Q _{gs}	Gate Source Charge		-	1.4	-	nC
Q _{gd}	Gate Drain ("Miller") Charge		-	1.7	-	nC
Switching Characteristics						
t _{d(on)}	Turn-On DelayTime	V _{GS} = -4.5V, V _{DD} = -15V I _D = -3A, R _{GEN} = 3Ω	-	10	-	ns
t _r	Turn-On Rise Time		-	86	-	ns
t _{d(off)}	Turn-Off DelayTime		-	150	-	ns
t _f	Turn-Off Fall Time		-	357	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	-4	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-16	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _S = -4A	-	-	-1.2	V
t _{rr}	Body Diode Reverse Recovery Time	I _F = -3A, di/dt = 80A/us	-	36	-	ns
Q _{rr}	Body Diode Reverse Recovery Charge		-	5	-	nC

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. R_{θJA} is measured with the device mounted on a 1inch² pad of 2oz copper FR4 PCB
 3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 0.5%.

Typical Performance Characteristics

Figure 1: Output Characteristics

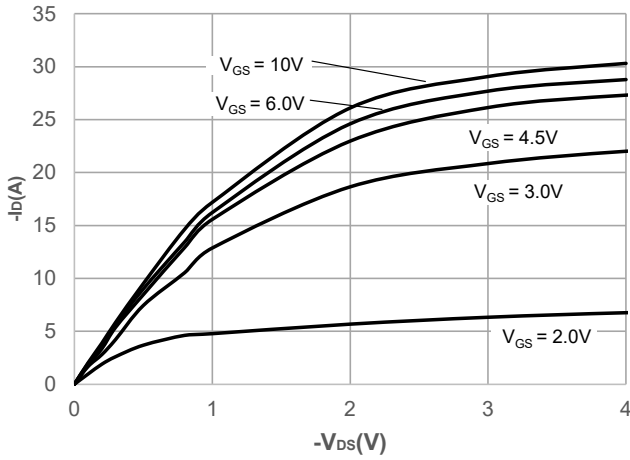


Figure 2: Typical Transfer Characteristics

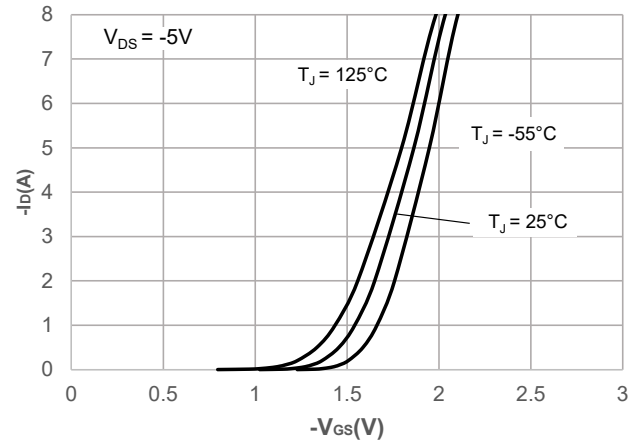


Figure 3: On-resistance vs. Drain Current

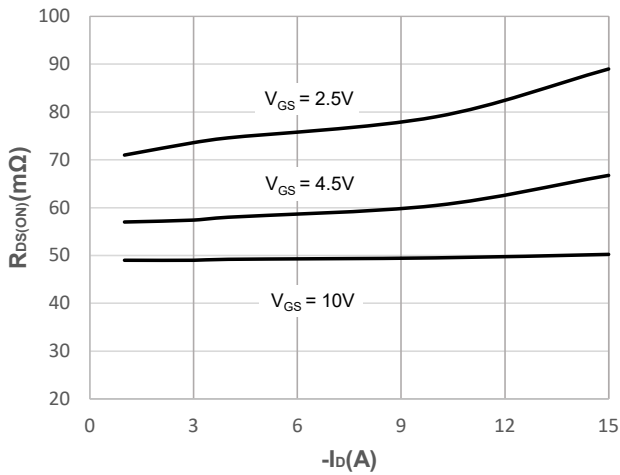


Figure 4: Body Diode Characteristics

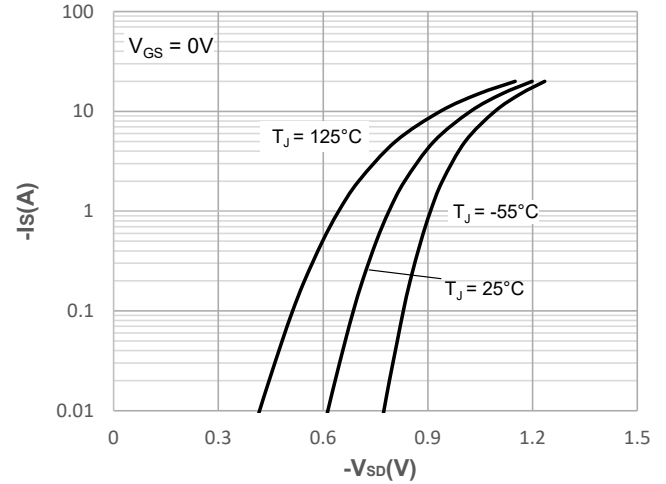


Figure 5: Gate Charge Characteristics

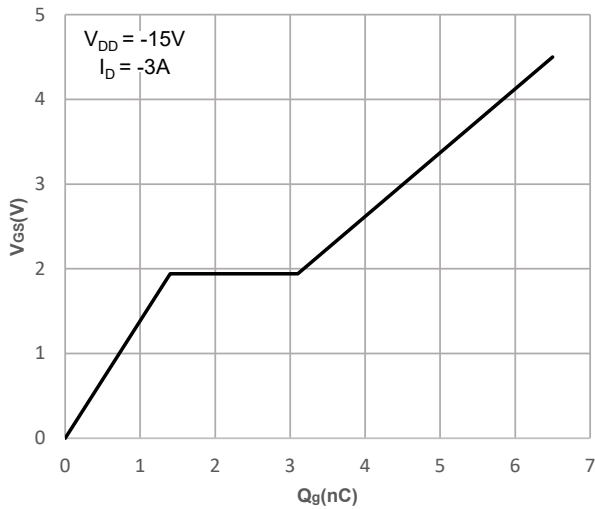
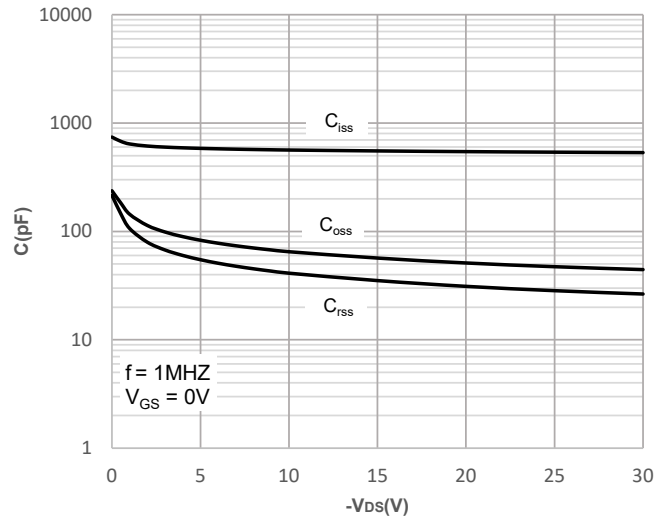


Figure 6: Capacitance Characteristics



Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

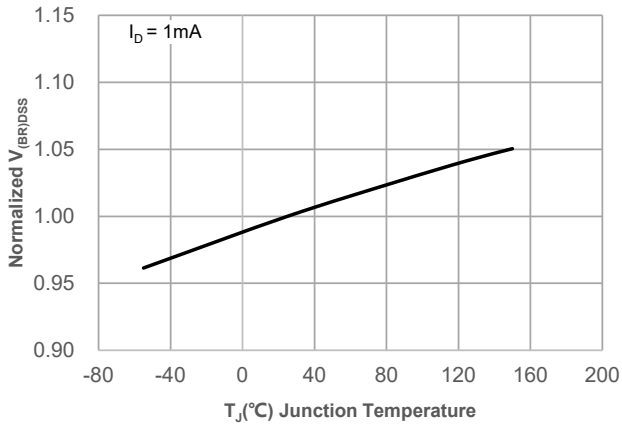


Figure 8: Normalized on Resistance vs. Junction Temperature

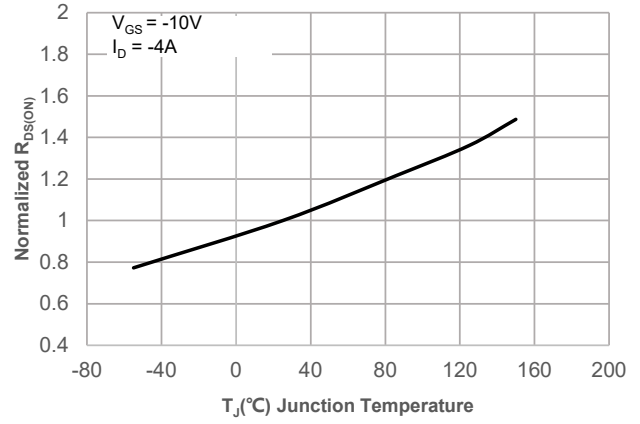


Figure 9: Maximum Safe Operating Area

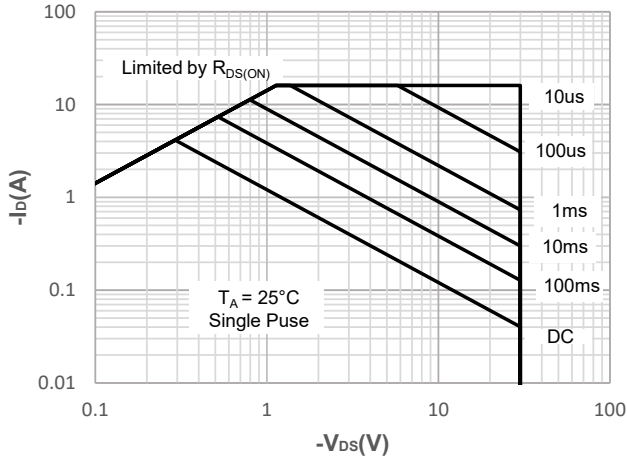


Figure 10: Maximum Continuous Drianc Current vs. Ambient Temperature

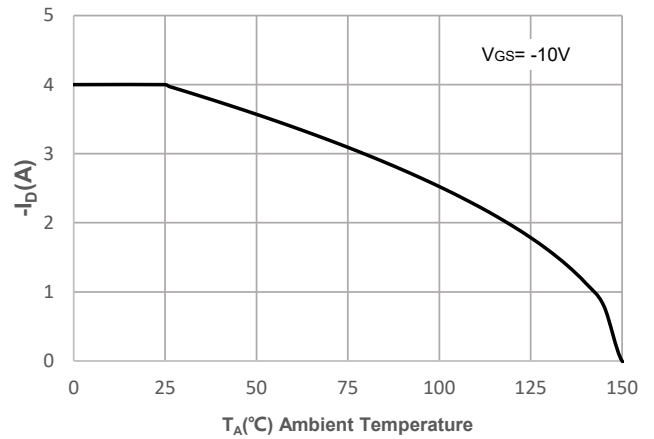


Figure 11: Normalized Maximum Transient Thermal Impedance

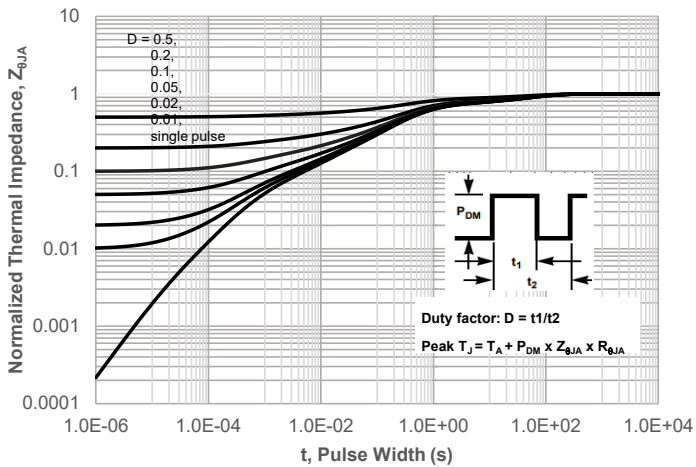
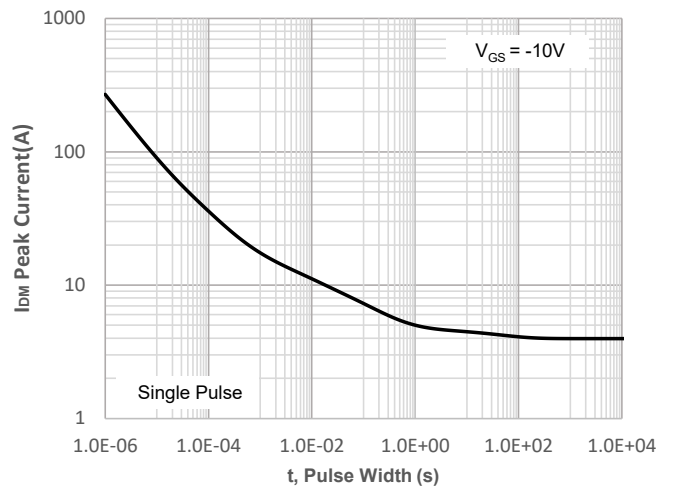


Figure 12: Peak Current Capacity



Test Circuit

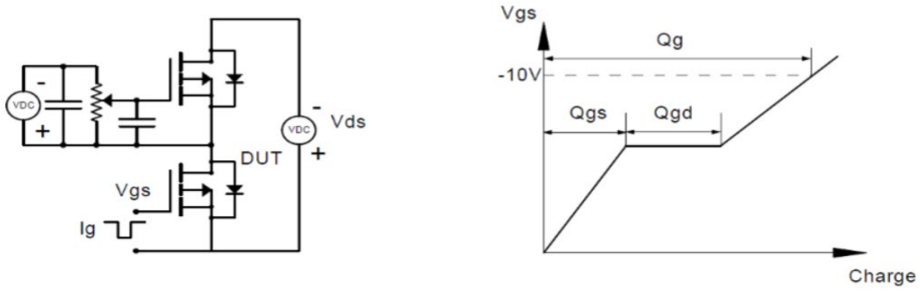


Figure 1: Gate Charge Test Circuit & Waveform

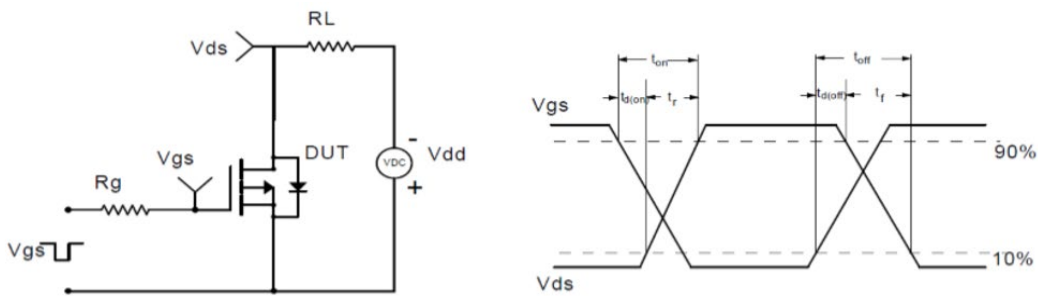


Figure 2: Resistive Switching Test Circuit & Waveform

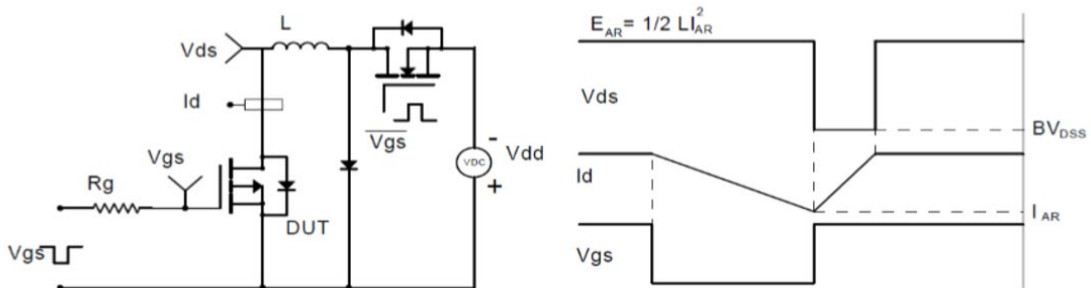


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

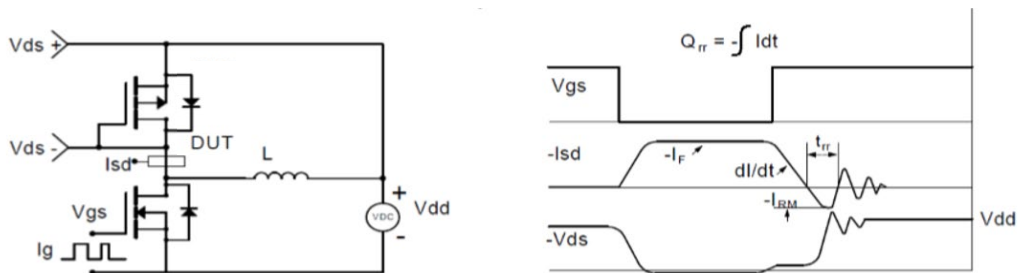
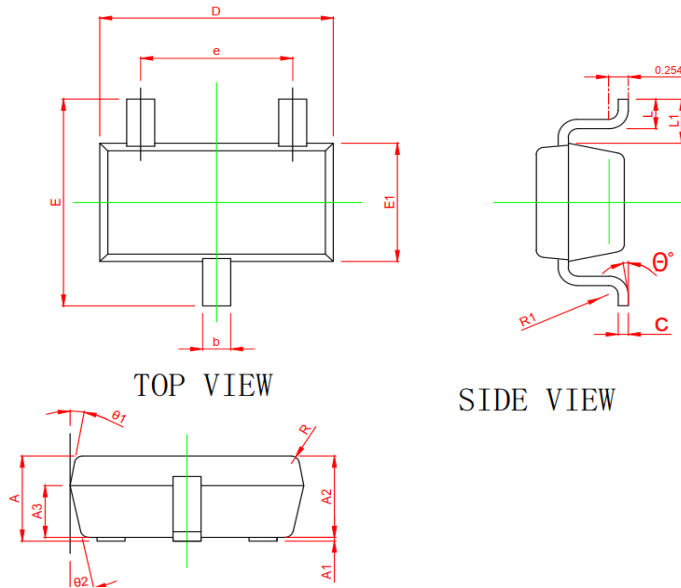


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(SOT-23-3L)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.25
* A1	0.02	-	0.10
* A2	1.05	1.10	1.15
A3	0.65	0.70	0.75
* b	0.30	0.35	0.45
* c	0.127 BSC		
* D	2.87	2.92	2.97
* E	2.72	2.80	2.88
* E1	1.55	1.60	1.65
* e	1.85	1.90	1.95
* L	0.32	0.40	0.48
* L1	0.55	0.60	0.65
R	0.10 REF		
R1	0.12 REF		
* θ	0	--	8°
θ_1	8°	10°	12°
θ_2	10°	12°	14°

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